#5

ADTST.031AUS

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Hiroaki Yamoto et al.	) Group Art Unit
Serial No.	:	09/941,396	)
Filed	:	August 28, 2001	)
For	:	METHOD FOR DESIGN VALIDATION OF COMPLEX IC	)
Examiner	:	Unknown	)

OIPE JC17
NOV 26 2001
PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

Enclosed is a form PTO-1499 listing the following two references relevant to the above-identified application.

(1) "Reuse Methodology Manual for System-on-a-Chip Design" and (2) "System-on-a-Chip: Design and Test", both of which are mentioned at page 1, lines 16-27 in the specification of the above-identified application.

Applicant respectfully requests that the Examiner consider the reference disclosed in the statement.

Respectfully submitted,

MURAMATSU & ASSOCIATES

Dated: 11/14/2001

By: Yasuo Muramatsu

Yasuo Muramatsu
Registration No. 38,684
Attorney of Record
7700 Irvine Center Drive
Suite 225, Irvine, CA 92618
(949) 753-1127

IDS-AD31.001
111301

Please type a plus sign (+) inside this box → ☐

PTO/SB/08B (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U. S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/941,396
Filing Date	8/28/2001
First Named Inventor	Hiroaki Tamoto
Group Art Unit	
Examiner Name	
Attorney Docket Number	ADTST.031 AUS

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Michael Keating "Reuse Methodology Manual", 1999, PP1~9 and PP229~251, Kluwer Academic Publishers	
		Rochit Rajsuman "System-on-a-Chip: Design and Test" PP1~31, PP125~153, 2000 Artech House	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.